



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/667,528	09/22/2000	Raimund Sonning	2789-26	9877
23117	7590	12/29/2004	EXAMINER	
NIXON & VANDERHYE, PC 1100 N GLEBE ROAD 8TH FLOOR ARLINGTON, VA 22201-4714			BAYARD, EMMANUEL	
			ART UNIT	PAPER NUMBER
			2631	

DATE MAILED: 12/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/667,528

Applicant(s)

SONNING ET AL.

Examiner

Emmanuel Bayard

Art Unit

2631

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 22 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-34 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 9,10,23 and 24 is/are allowed.
- 6) ☒ Claim(s) 1-8,11-22 and 25-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date: _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date: _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 12 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.
3. Claim 12 recites the limitation "said decoded code " in lines 2-3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 4, 6-7, 11-12, 13, 15, 17-19, 25, 28, 30-34 are rejected under 35 U.S.C. 102(b) as being anticipated by Alanara et al U.S. Patent No 5,594,797.

As per claims 1, 11, 13, 18-19 Alanara et al teaches an interleaver of a transmitter for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits and control information associated with every code symbol to be used to control processing

Art Unit: 2631

in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol comprising: a channel coder is the same as the claimed (channel encoder) (see fig.1 element 132 and col.4, lines 43-45) for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits; An adder is the same as the claimed (combining means for combining) (see fig.4 element 350 and col.8, lines 40-54) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of $L + N$ bits; control information/code symbol **encoding means** (see fig.1 element 116 and col.3, lines 21-30 and col.6, lines 17-23) for encoding said $L + N$ bit control information/code symbol data words into data words of K bits, where $K < L + N$, according to a predetermined encoding scheme; an interleaving memory for storing (see fig.1 element 136) said encoded data words at memory locations thereof.

As per claims 4, 17 the interleaver of Alanara teaches a power off (see col.6, lines 37-38). Therefore a transmission power on/off is inherently includes in Alanara.

As per claim 6, the interleaver of Alanara does teach a convolutional encoding having a coding rate (see col.3, lines 50-51).

As per claim 7, the interleaver of Alanara does teach interleaving ROM memory (see col.3, lines 26-27). Therefore the ROM memory inherently includes number of rows and columns.

Art Unit: 2631

As per claim 12, the transmitter of Alanara does teach a modulation means (see col.5, lines 22-25).

As per claim 15, the method of Alanara does include a processing decoded code (see fig.1 element 160).

As per claims 25 and 33, Alanara teaches Alanara et al teaches an interleaver of a transmitter for interleaving input data bit sequences (BS) of M data bits comprising code symbols each consisting of a number N of data bits and control information associated with every code symbol to be used to control processing in said transmitter and consisting of a number L of control bits indicating specific states for each corresponding code symbol comprising: a channel coder is the same as the claimed (channel encoder) (see fig.1 element 132 and col.4, lines 43-45) for receiving digital data in the form of packets from a data source and for encoding said digital data into said channel encoded code symbols of said number N of data bits; An adder is the same as the claimed (combiner) which combines (see fig.4 element 350 and col.8, lines 40-54) the respective data bits of each code symbol with the associated L control bits into a control information/ code symbol data word of L + N bits; control information/code symbol **encoding means** (see fig.1 element 116 and col.3, lines 21-30 and col.6, lines 17-23 and col.7, lines 43-44) for encoding said L + N bit control information/code symbol data words into data words of K bits, where $K < L + N$, according to a predetermined encoding scheme; an interleaving memory for storing (see fig.1 element 136) said encoded data words at memory locations thereof; a decoder (see fig.1 element 160 and col.4, line 22 and col.5, line 61)

Art Unit: 2631

which derives the control information from the data words; a radio frequency transmitter element (see fig.1 element 140 and col.5, line 21) whose operation is controlled by the controlled information derived from the decoder.

As per claim 28 the interleaver of Alanara teaches a power off (see col.6, lines 37-38). Therefore a transmission power on/off is inherently includes in Alanara.

As per claim 30 the interleaver of Alanara does teach a convolutional encoding having a coding rate (see col.3, lines 50-51).

As per claim 31 the interleaver of Alanara does teach interleaving ROM memory (see col.3, lines 26-27). Therefore the ROM memory inherently includes number of rows and columns

As per claims 32 and 34 the method of Alanara does include a radio frequency transmitter (see col.5, line 21).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2-3, 5, 8, 14, 16, 20-22, 26-27, 29 rejected under 35 U.S.C. 103(a) as being unpatentable over Alanara U.S. patent No 5,594,797 in view of Hatakeyama et al U.S. patent No 6,507,629 B1.

Art Unit: 2631

As per claims 2, 8, 14, 26 Alanara teaches all the features of the claimed invention except write/read means for writing said encoded data to an interleaving matrix having row and column directions.

Hatakeyama teaches teach write/read means in row and column directions (see abstract and figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col. 12, lines 48-55 and col. 14, lines 10, 22 and col. 15, line 48 and col. 17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) and symbol decoding means (see fg.4 elements 13, 27 and col.9, line 41 and col. 10, line 12). Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving Matrix is inherently taught by Hatakemaya.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hatakeyama into Alanara as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

As per claims 3, 16 and 27 the interleaving of Hatakemaya does teach a frame start, a power bit (seecol.3, lines 52-69 and col.24, lines 17-20, 50-55). Note that a frame is known in the art as plurality of time slot having a header, a maker. Since Hatakemaya teaches a frame function therefore the time slot start and a marker is inherently taught by Hatakemaya. Furthermore implementing such teaching into Alanara would have been obvious to one skilled in the art as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

As per claims 5, 29, the interleaver of Hatakemaya does teach a selection means of write/read means (see abstract). Furthermore implementing such teaching into each memory location of Alanara reference would have been obvious to one skilled in the art as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

As per claims 20-22, Alanara teaches all the features of the claimed invention (see claims 1 and 25 above) except write/read means for writing said encoded data to an interleaving matrix within said interleaving memory at specific memory location in a row direction and for reading out said encoded data words from said interleaving matrix in the column direction.

Hatakeyama teaches teach write/read means in row and column directions (see abstract and figs.8, 9, 14, 17 elements 51, 52, 6, 10 and col. 12, lines 48-55 and col. 14, lines 10, 22 and col. 15, line 48 and col. 17, lines 15-20 and col.21, lines 53-58 and col.22, lines 2-6, 21-25) and symbol decoding means (see fg.4 elements 13, 27 and col.9, line 41 and col. 10, line 12). Note that a matrix is known in the art as function having Rows and column. Since the interleaver of Hatakemaya teaches Rows and column therefore the interleaving Matrix is inherently taught by Hatakemaya.

It would have been obvious to one of ordinary skill in the art to implement the teaching of Hatakeyama into Alanara as to reduce the memory capacity required to for interleave processing as taught by Hatakeyama (see col.4. lines 19-20).

Allowable Subject Matter

Art Unit: 2631

Claims 9-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 23-24 are allowed over the prior art of record.

The following is a statement of reasons for the indication of allowable subject matter: a shift means for shifting the register (r0, r1) which was read at the last write cycle and the second registers of the register banks (b0, b1) while reading in the next odd and even bits of a next input data bit sequence to the respective second register (r1) of each register bank as recited in claims 8-10 and 23-24.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emmanuel Bayard whose telephone number is 571 272 3016. The examiner can normally be reached on Monday-Friday (3:PM-10:PM) Alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammed Ghayour can be reached on 571 272 3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2631

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Emmanuel Bayard
Primary Examiner
Art Unit 2631

12/21/04



EMMANUEL BAYARD
PRIMARY EXAMINER